

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)	
)	
Hisataka MEGURO et al.)	
)	Group Art Unit: Not assigned
Serial No.: Not Yet Assigned)	
)	Examiner: Not assigned
Filed: September 29, 2003)	
)	
For: SEMICONDUCTOR MEMORY)	
DEVICE)	

**Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450**

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§1.56 and 1.97(b), applicants bring to the Examiner's attention the documents listed on attached Form PTO-1449. Copies of the listed documents are attached. Applicants respectfully request that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form.

This Information Disclosure Statement is being filed with the above-referenced application.

The following is a concise statement of relevance of the non-English language documents:

1. Japanese Patent Application No. 2002-57227 discloses a semiconductor memory device characterized by bit line contact consisting of two or more wiring layers.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

The relevance of this document is discussed at page 3 of the specification of the present application. An English-language abstract of the document is also enclosed.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicants determine that the cited documents do not constitute "prior art" under United States law, applicants reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents. Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.



By: 

Richard V. Burgujian

Reg. No. 31,744

ERNEST F. CHAPMAN

Reg. No. 25,961

Dated: September 29, 2003

Enclosures
RVB/FPD/dvz

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	02887.0252	Serial No.	
Applicant	Hisataka MEGURO et al.		
Filing Date	September 29, 2003	Group:	Not assigned

U.S. PATENT DOCUMENTS							
Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
		5,356,834	10/18/94	Sugimoto et al.			
		5,994,218	11/30/99	Sugimoto et al.			

FOREIGN PATENT DOCUMENTS							
		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
		2002-57227	2/22/02	Japan			Abstract

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	Shirota, R. et al., "Nonvolatile Semiconductor Memory Device and Method of Manufacturing the Same", Serial No. 09/470,518, filed December 22, 1999.

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce